The Effect of Integration of Strontium-Bismuth-Tantalate Capacitors onto SOI Wafers.♣

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We report for the first time the successful integration of Strontium-Bismuth-Tantalate ferroelectric capacitors on an SOI Substrate. We have verified that the unique processing requirements of SBT capacitors does not affect the properties of the surrounding FD-SOI transistors, and, conversely, we have verified that the SOI processing does not affect the quality of the SBT capacitors.

Motiviation

The integration of SBT capacitors on SOI substrate was borne out of a request by NASA's Jet Propulsion Laboratory to develop a suitable replacement for a non-volatile memory element used for start-up/boot-up code for a processor selected for use on the Prometheus Deep Space mission.

The use of SOI was considered a natural selection due to its well known capabilities in terms of operation through and after exposure to intense ionizing radiation fields.[1] The use of SBT capacitors as data storage elements was also a natural selection due to its well-known improved performance and processability when compared to other materials, such as PZT (Lead-Zirconium-Tantalate).[2]

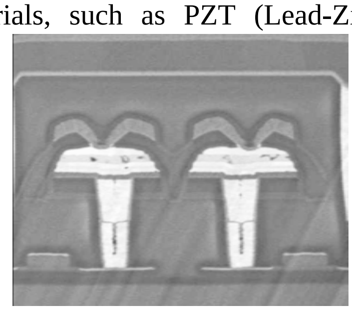

Figure 1: Fully integrated SBT capacitors on FD-SOI

For this development, Metal Organic Decomposition (MOD) SBT solution commercially available from Kojundo Chemicals, Japan was applied to Unibond SOI wafer by Oki Electric Industry at their Hachiouji fab. The technology chosen was Oki's 0.2 µm scale FD-SOI transistors.

Novelty

We have, for the first time, succesfully integrated ferro-electric capacitors of any type (in this case, SBT) onto SOI substrate by overcoming several factors, namely the etching of very-deep tungsten plugs with an aspect ratio of 5.5 on ultra-thin S/D region (50 nm) , the development of two-step plugs under ferroelectric capacitor without the use of an interstitial pad in order to mitigate the stress to ultra thin SOI, and the modification of the SBT capacitor formation temperature profile resulting in elimination of an increase in back-channel leakage.

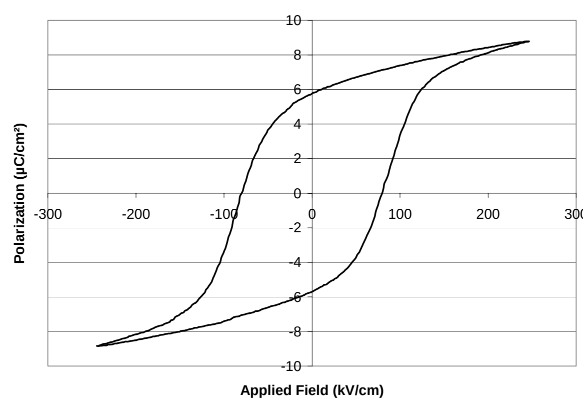

Figure2: Hysteresis of an integrated SBT capacitor(2 µm²) on FD-SOI

♣ This development funded, in part, by NASA's Jet Propulsion Laboratory, Pasadena, California, under contract 1265898, in support of NASA Task Order 7107141 and the NASA Prometheus Program.

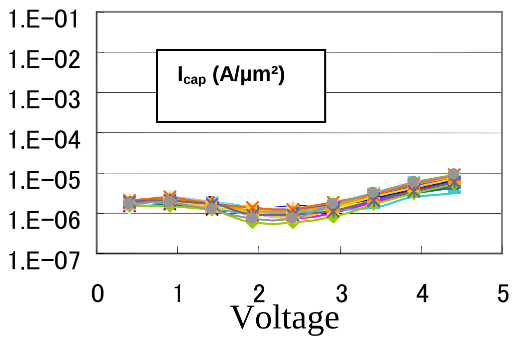

Figure 3: Leakage of an integrated SBT capacitor(2 µm²) on FD-SOI. Multiple point test.

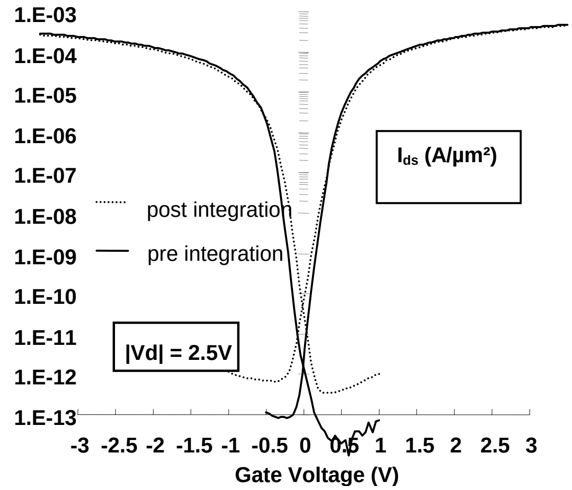

Figure 4: Comparison of Ids-Vgs curves of FD-SOI transistors (0.35 x 10 µm) with and without SBT capacitors.

Device Peformance

Figure 2 and 3 show the characteristics of SBT ferroelectric capacitors fully integrated into 0.2 µm FD-SOI with three layers of metallization, nitride passivation, and $CoSi_2$ contact process. The SBT film thickness is 120 nm. As can be seen, good hysteresis loops with excellent leakage characteristics are obtained on these integrated capacitors thus qualifying them for memory operation. Figure 4 shows the Ids-Vg characteristics of SOI transistors. The two plots compare the transistor characteristics with and without SBT capacitor integration. The data confirms that integration process of SBT capacitor has negligible effect on the SOI transistor characteristics and thus FD-SOI transistors can be integrated with SBT ferroelectric capacitors for ultra high speed and ultra low power non-volatile memory fabricaton.

Total Ionization Dose

The TID testing of FD-SOI transistors, post integration, is currently being carried out. We will present that information and compare that to data obtained earlier from TID testing of 0.2 µm FD-SOI transistors. The devices were sybject a total ionization (gamma) radiation to a level of 300 kRads (Si).

For this purpose a test chip was designed with numerous transistor varying in the width-to-length ratio. Strutures with the use of body ties and enclosed body architecture to control cell leakage were also designed.

Conclusion

We have shown that SBT ferroelectric capacitors can be successfully integrated onto FD-SOI wafer with no degradation in either leakage or capacitor performance. We have shown that the process challenges of etching of deep tungsten plugs with large aspect ratios on ultra-thin Si is possible and finally we have shown processes specific to ferroeletric capacitor do affect the FD-SOI transistor characteristics. The radiation effects on FD-SOI transistors, post integration, are under investigation.

Future Developments

With the proof-positive that one can succesfully integrate SBT ferroelectric capacitors onto SOI with no deletrerious effect on either, opens the door to a new generation of memory devices for almost any practical use: from wristwatches and cell phones to deep space missions, the Holy Grail of non-volatility, low power, high speed and high radiation immunity is, at once, achieved.

References

[1] Mitsubishi Heavy Industry and JAXA, "SEE characteristics of 0.2 µm FD-SOI SRAM," Presentation IRPS, 2004

[2] C. A. Araujo, J. D. Cuchiaro, M. Scott, L.D. McmIllan, "Fatigue free properties of SBT on Pt electrodes," Nature, vol. 374, pp. 627, 1995